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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/693,157	10/20/2000	Jang-Ho Cho	SAM-162	8192

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EXAMINER
GERSTL, SHANE F

ART UNIT	PAPER NUMBER
2183	3

DATE MAILED: 08/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/693,157	CHO, JANG-HO	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2000 and 23 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☒ Claim(s) *1 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☒ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

The faxed copy is incomprehensible. The examiner cannot make a sound judgment as to its correctness. Please submit another copy.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Multi-level Pattern History Branch Predictor Using Branch Prediction Accuracy History to Mediate the Predicted Outcome.

3. The disclosure is objected to because of the following informalities:

a. The headings of each section should not be underlined as described in 37 CFR 1.77(c).

b. On page 6, line 12 mentions a "pattern history bit." Claim 2 refers to "pattern history bits" rather than a single bit, as does Figure 2. The examiner is interpreting this phrase to say, "pattern history bits." There are many instances of a "pattern history bit" such as that mentioned throughout the document and the one given is simply an example. The examiner requests that all inconsistencies be remedied.

c. On page 2, line 27 the applicant makes reference to a publication called "MOCROPROCESSOR." The cited reference should be "MICROPROCESSOR REPORT," reflecting the spelling mistake and the entire publication name. Appropriate correction is required.

d. The applicant makes mention of "the most recent k conditional branches" on pages 5-6, lines 29-1. It is requested that clarification is made on whether the invention makes of use of the actual most recent k conditional branches or the most recent k occurrences of the same conditional branch. Both of these implementations are discussed by Yeh and Patt. Gwennap discusses the use of the most recent k occurrences of the same conditional branch using a branch history register for each instruction. The examiner is interpreting the applicant's disclosure to mean the actual most recent k conditional branches, regardless of type based on claim 2 where a single branch history register is used. Appropriate correction is required.

Drawings

4. The drawings are objected to because Figure 2 makes mention of "Accuracy History Bits" when everywhere else in the disclosure and claims the phrase "accuracy history bit" is used indicating the use of a single bit. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 8 is objected to because of the following informalities: line 2 mentions the "most significant bit of the accuracy history bit". The examiner requests that this be changed to simply "the accuracy history bit" since the most significant bit of a bit is simply that bit.

Appropriate correction is required.

6. Claim 1 is objected to because of the following informalities: the claim can be interpreted to have multiple embodiments if one does not consider the specification and drawings. Page 9, line 4 refers to "a conditional branch" which can be viewed as having multiple meanings. The examiner is interpreting this "conditional branch" and the one of line 11 to mean the prediction output of the branch prediction means. The examiner suggests that this signal be conveyed in both places in a clearer manner so as to adequately illustrate the intent such as calling this "conditional branch" a "conditional branch prediction".

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Manne in view of Hennessy. Manne's Paper "Branch Prediction using Selective Branch Inversion," (International Conference on Parallel Architectures and Compilation

Techniques, 1999) describes how accuracy history can be combined with multiple branch prediction schemes.

In regard to claim 1:

a. Manne teaches a branch predictor (SBI Predictor) as seen in Figure 1. Note Manne's branch prediction means for predicting a conditional branch of a branch instruction (Figure 1, Branch Predictor). Refer to section 2.2, paragraph 1, lines 16-18 where Manne discloses a branch being correctly predicted. A comparator would have been used to determine if the branch was correctly predicted. This makes a comparator for generating a comparison signal by comparing the predicted conditional branch from the branch prediction means with a real conditional branch of the branch instruction inherent. Manne also discloses an accuracy history table (confidence estimator of Figure 1) for storing an accuracy history of the predicted conditional branch. Note Manne's use of a first state transition logic circuit (section 4.1, paragraph 2, one-bit resetting counter) for generating an accuracy history bit to be stored in the accuracy history table in response to the comparison signal.

b. Manne lacks the explicit use of a multiplexer for outputting an alternative one of the conditional branch and an inverted conditional branch as a final branch prediction outcome, in response to a predicted accuracy history signal based on the accuracy history bit.

c. However, Manne does teach that the branch prediction is inverted for all low-confidence branches. Therefore, the Selective Branch Inversion predictor

(Manne, Figure 1) would output either the conditional branch from the branch predictor or an inverted conditional branch from the branch predictor as a final branch prediction result.

d. As demonstrated by Hennessy on page 351, a multiplexer is usually used in a system to select among inputs to share a data path because of its simplicity of design and integration. This simplicity leads to low cost and good performance. The simplistic design and integration would have motivated one with ordinary skill in the art at the time of invention to use a multiplexer in Manne's proposal for outputting an alternative one of the conditional branch and an inverted conditional branch as a final prediction output.

It would have been obvious to one with ordinary skill in the art at the time of invention to use a multiplexer to select the correct data for the final branch prediction outcome so that the integration of the system is simple and efficient.

In regard to claim 2, note that the Gshare predictor of Figure 2a can be used as the branch predictor portion of Figure 1. Manne discloses the use of a branch history register for storing the outcome of previous branch instructions as described in section 2.1, paragraph 2. The two-bit counter scheme, a standard in the Gshare predictor, of section 2.1, paragraph 2 serves as a second state transition logic circuit for generating the pattern history bits in response to the real conditional branch of the branch instruction. Also note, Manne's use of a pattern history table (Figure 2a) for storing pattern history bits used for generating the predicted conditional branch corresponding

to the conditional branches of the previous branch instructions stored in the branch history register in this embodiment.

In regard to claim 3, notice Manne's use of a two-bit counter on paragraph 4 of section 4.1 that is included in the second state transitional logic of the standard Gshare algorithm. This counter is by nature up/down counting so the pattern history can change based on both a taken and not-taken branch. The counter in this algorithm is also of the saturating type so that a counter of the strong taken state does not roll over to the strong not-taken state because of another taken branch.

In regard to claim 4, note Manne's use of an accuracy history table as explained previously. This table keeps track of, or stores, a number of correct predictions. This in itself defines memory since it is holding data for later retrieval. This accuracy history table also is an arrangement of such elements, or an array. Thus Manne's accuracy history table does include a memory array.

In regard to claim 6, Manne keeps a count of correct predictions in his accuracy history table using a first state logic circuit that includes a saturated up/down counter (paragraph 4 of section 4.1).

In regard to claim 5, the saturating counter of the above argument requires a different value to be received from the inherent comparator discussed above for a correct prediction than an incorrect prediction. A '1' will increase the count by one and a '0' decrease it, or visa versa. If a different value is not given for correct or incorrect, the counter will eventually be stuck at either the upper or lower extremities with no way to count in the other direction.

In regard to claim 7, this first state logic counter will be used after learning the accuracy of past pattern predictions since the comparator output is the activating signal and it determines if the past predictions were correct or not.

In regard to claim 8, since the accuracy history bit is only one bit, the most significant bit thereof is one and the same with it. Therefore the predicted accuracy signal, which is determined by the accuracy history bit will also be determined by the most significant bit of the accuracy history bit.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The following patents are cited to further show the art with respect to multi-level branch prediction comprising accuracy and up/down saturating counters with history tables in general.

US Pat. No. 6,055,629 to Kulkarni et al. shows a method for prediction correlation between a first group of branch instructions in a bunch and a second group of branch instructions in a bunch.

US Pat. No. 6,484,256 to Levitan et al. shows a branch prediction scheme comprising multiple tables.

US Pat. No. 5,564,118 to Steele et al. discloses a microprocessor including a past-history filtered branch prediction method.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (703)305-7035. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703)305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)305-3900.

Shane F Gerstl
Examiner
Art Unit 2183

SFG
August 19, 2003

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